VENTANA MICRO BRINGS RISC-V INTO THE DATA CENTER

The data center is becoming more heterogeneous in terms of customized processors, accelerating new workloads across the infrastructure to optimize data movement, computation, and security. Ten years ago, the Smart-NIC started this revolution, with Arm finding a spot on the top of the AWS rack. Now, every corner of the infrastructure landscape is getting smart, creating opportunities for ASICs, FPGAs, GPUs, and CPUs to carve out a spot and build an ecosystem.

Five years ago, many surmised that Arm cores would address most of these opportunities. But now, that's not how we see it playing out. The rise of RISC-V as a viable and flexible technology is undeniably helped by the open-source platform's excellent fit as the CPU in a multi-chiplet architecture enabling innovation without the limiting constraints of Arm licensing terms.

A few years back, a team of designers and leaders at Applied Micro decided that it was time for RISC-V to literally grow up and achieve performance on par with X86 and Arm. Many had worked together at Veloce, which was later acquired by Applied Micro (AMCC) where they created the first 64-bit Arm server. This team, now with Ventana, drove much of the data center architecture and ecosystem for Arm and are uniquely qualified to repeat that for RISC-V. Not surprisingly, they have now raised nearly \$100M in capital at Ventana Micro.

"Ventana is leading the market in bringing high performance RISC-V CPU cores and cutting edge chiplet solutions to the Data Center, Edge, 5G, Automotive and Client markets," said Balaji Baktha, founder and CEO of Ventana Micro Systems. "Over the past few years, we have been laser focused on ensuring that the RISC-V ecosystem is mature for data center class workloads and are happy to report commercialization with hyperscale customers in 2023."

A key motivation for RISC-V is the emergence of a wide range of domain-specific accelerated components across the infrastructure. A more friendly licensing model is excellent; a high-performance CPU core is better. But



Balaji Baktha, Ventana Micro CEO

having a partner to help build a collaborative SoC design is pivotal to success. Emerging chiplet IP and chip integration technologies allow companies to develop their



semi-custom solution on top of proven RISC-V cores and I/O hub IP. This trend will enable companies to concentrate their efforts on value-added and differentiated IP and accelerate time to value at a lower cost. As the industry moves to a composable semiconductor model based on chiplets, a new wave of companies will emerge to offer IP to the broader industry. We believe this will accelerate innovation.

VENTANA'S VALUE PROPOSITION

Ventana Microsystems, a Bay-Area startup, has emerged as the leading contender to own this space or take an early lead. The company has created a high-performance RISC-V IP, which can form a flexible and extensible CPU for various data center infrastructure applications. The company sees this as a surprisingly ample opportunity, totaling over \$90B in TAM across data center infrastructure (not including server CPUs), automotive, 5G, networking and storage, and AI accelerators. Let's examine why we believe they are well positioned for leadership and will attract many partners to build solutions.

But first, let's dispel the myth that RISC-V is not up to the performance demands of the data center. The Ventana core delivers 425-500 SPEC CPU Int, which puts it in the same class as an AMD Epyc Genoa server CPU and brings RISC-V into a competitive position concerning x86 and Arm. The Ventana processor can support integrations with standard third party AMBA-based IP. That, combined with server-class performance, means there are no real limitations for anyone taking this technology into the server space.

Ventana Microsystems will initially focus on data center infrastructure solutions. Ventana and the RISC-V software community have already demonstrated the ability to run many open-source cloud-native applications. Software is much further along in the RISC-V world than they were for Arm at this early stage. Many applications with architecture dependencies were made ISA portable during their move to Arm, so things are much easier to port this time.

The advantage to Ventana customers is significant, allowing them to shave months or even years off their schedule by building on the tested foundation that Ventana provides. Based on demand for leadership performance, the company intends to foster HW/SW co-design projects with its clients, enabling customer innovation through the extensible RISC-V ISA and providing the technology and support to build custom multi-chiplet heterogeneous architectures. Ventana and its partners are already exploring networking, storage, security, and load-balancing solutions.



VENTANA **Chiplets Accelerate TTM and Maximize ROI** Ventana Accelerator Chiplet Compute Chinlets Accelerator Compute CHI-based Coherent CHI-based Coherent On-chip Interconnect **On-chip Interconnect** DDR5 DDR5 DDR5 DDRS PCIe Gen4/5 PCIe Gen4/5 Monolithic SoC **Chiplet-based SoC** TTM: 3+ years TTM: < 1 year Development cost: \$100M+ Development cost: < \$20M Leading edge process node Each chiplet in optimal process node Fixed performance Scalable Compute, Accelerator and I/O performance

Figure 1: Ventana believes it can shave years off the development time of a custom ASIC.

For Die-to-Die interconnects, Ventana plans to support both BoW (Bunch of Wires) and the Universal Chiplet Interconnect Express (UCIe) standard supported by Intel, AMD, NVIDIA, Arm, and others. In addition, Ventana has recruited support from a dozen IP/chiplet partners to deliver turnkey solutions for chiplet-based solutions, along with a robust SDK including firmware, BIOS, OS, reference applications for storage and networking, and a BMC.

Ventana also makes its CPU core IP available to clients who want to build a complete ASIC on top of a proven CPU design. In both models, Ventana sees applicationsspecific accelerators dovetailing nicely. Finally, Ventana offers clients a flexible engagement model, including IP for SoC integrated turnkey solutions, or can interface a compute chiplet to a client's custom I/O hub.

CONCLUSIONS

The age of chiplets is dawning rapidly, concurrently with the emergence of highperformance RISC-V CPUs offering attractive extensions and customization terms. Combined, this seems like a perfect storm that will spur innovation and form new companies. Ventana Microsystems is well positioned to capitalize on these two megatrends in the semiconductor industry.

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IMPORTANT INFORMATION ABOUT THIS PAPER

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